IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Hideaki Kuwabara et al.	Art Unit :	2822
Serial No.	: 10/735,767	Examiner :	Kevin Picardat
Filed	: December 16, 2003	Confirmation No.:	4086
Title	: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME		

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INTERVIEW SUMMARY AND REPLY TO ACTION OF APRIL 7, 2006

In response to the non-final office action of April 7, 2006, applicant asks that all claims be allowed in view of the following remarks. Claims 11-12, and 14-31 are currently pending, of which claims 11, 15, 18, 21 and 29 are independent.

Applicant would like to thank Examiner Picardat for the courtesies extended to applicant's representative during the telephone interview conducted on August 3, 2006. As reflected in this reply, the Examiner indicated citations in the applied art where the Examiner asserted the elements of independent claims 11, 15, 18, 21 and 29 were disclosed.

Applicant acknowledges with appreciation the Examiner's indication that claims 14, 17, 20, 22 and 31 would be allowable if written in independent form including all limitations of the base claim and any intervening claims. Applicant has not amended these claims at this time.

Claims 11, 12, 15, 16, 18, 19, 21, 24, 26, 29 and 30 been rejected as being unpatentable over Sayyah (U.S. Patent No. 6,589,811) in view of Ding (U.S. Patent No. 6, 737,300). Applicant requests reconsideration and withdrawal of this rejection because neither Sayyah, Ding, nor any proper combination of the two, describes or suggests dividing the element layer into at least one integrated circuit film, as recited in each of independent claims 11, 15, 18, 21 and 29, and for the additional reasons set forth below.

Claim 11 recites a method for manufacturing a semiconductor device that includes forming a crystalline semiconductor film over a first substrate. The method also includes forming an element layer that includes an element using the crystalline semiconductor film, a wiring for transmitting an electrical signal to the element, and an insulating film. The method further includes transferring the element layer from the first substrate to a second substrate,

transferring the element layer to a sheet, and dividing the element layer into at least one integrated circuit film.

As best understood, the Examiner indicates that Sayyah discloses, in "DEVICES/CIRCUITS 1" shown in Figs. 3a-3f and related text, forming a crystalline semiconductor film over a first substrate; forming an element layer that includes an element using the crystalline semiconductor film, a wiring for transmitting an electrical signal to the element, and an insulating film; transferring the element layer from the first substrate to a second substrate; and transferring the element layer to a sheet. The rejection indicates that Sayyah does not disclose dividing the element layer into at least one integrated circuit film, and relies on Ding's disclosure of cutting an individual chip scale package 100 from an assembly of multiple such chip scale packages for showing the step of dividing the element layer into at least one integrated circuit film, as recited in each of the independent claims. See Ding at FIGS. 13-14; col. 3, lines 1-37; and col. 4, line 66 to col. 5, line 5. Ding's individual chip scale package 100 includes a substrate attached to the active surface of a semiconductor chip 130 through an anisotropic conductive adhesive film 120 and multiple contact pads 110a provided with the lower surface of the substrate 110.

However, Ding's disclosure of cutting an individual chip scale package cannot be properly combined with Sayyah's method of forming a semiconductor device, as one skilled in the art would not have been motivated to combine the cutting method of Ding with Sayyah's method of forming a semiconductor device. Nothing in Ding or Sayyah would have provided motivation to incorporate Ding's cutting of individual chip scale packages with Sayyah's method of forming a semiconductor device. Contrary to assertions made in the rejection, allowing for a more reliable electrical connection between structures is not sufficient motivation for combining Ding with Sayyah, since there is no indication that such a reliable connection results from the cutting rather than from other aspects of Ding. Nor does the mere existence of a cutting method provide motivation to incorporate Ding's cutting of chip scale packages with Sayyah's method of forming a semiconductor device.

Moreover, while Ding describes cutting of individual chip scale packages, an individual chip scale package is not an integrated circuit film. As evidence of this, the specification points to the difference: "An integrated circuit film formed by a technique for transferring is a film

including a semiconductor layer with a thickness of from 30 nm to 60 nm, and is much thinner than a semiconductor chip." See specification at page 3, lines 4-6.

The action states: "Sayyah's disclosure does not disclose the entire end product and that some form of singulation must eventual [sic] take place and that Ding teaches a suitable method of dicing." See action at page 3. As noted above, applicant disagrees that the mere existence of a cutting method provide motivation to incorporate Ding's cutting of chip scale packages with Sayyah's method of forming a semiconductor device.

As such, Ding does not remedy Sayyah's failure to describe or suggest dividing the element layer into at least one integrated circuit film, as recited in independent claim 11.

In addition, Sayyah's film (2) (referred to as a sheet transfer layer 2) is not disclosed to be a crystalline semiconductor film, as recited by claim 11.

Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 11 and its dependent claim 12.

Claim 15 also recites a method for manufacturing a semiconductor device that includes forming a crystalline semiconductor film over a first substrate and dividing the element layer into at least one integrated circuit film. The method of claim 15 also includes forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring; transferring the element layer from the first substrate to a second substrate so as to dispose the protruding electrode between the second substrate and the element layer; forming a thermal conductivity film on the element layer; and transferring the element layer and the thermal conductivity film from the second substrate to a sheet.

As best understood, the Examiner relies on Ding's metal bump 140 in Figs. 2, 4 and 6 as corresponding to forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring, as recited in claim 15. The Examiner, as best understood, indicates that Ding in Figs. 13 and 14 show the metal bump 140 between two substrates and, as such, discloses transferring the element layer from the first substrate to a second substrate so as to dispose the protruding electrode between the second substrate and the element layer, also as recited in claim 15.

Ding discloses that "the metal bumps 140 on each substrate 110 are electrically coupled to corresponding bonding pads 130a on the chip 130." Ding at col. 4, lines 24-26. As such,

Ding's "metal bumps" do not disclose a protruding electrode. Hence, Ding does not describe or suggest in the cited portion, or anywhere else, forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring, as recited in claim 15. Because Ding does not describe or suggest the claimed protruding electrode, Ding necessarily cannot describe or suggest transferring the element layer from the first substrate to a second substrate so as to dispose the protruding electrode between the second substrate and the element layer, as also recited in claim 15.

As such, Ding does not remedy Sayyah's failure to describe or suggest forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring or transferring the element layer from the first substrate to a second substrate so as to dispose the protruding electrode between the second substrate and the element layer, as recited in claim 15.

In addition, as described above with respect to claim 11, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests dividing the element layer into at least one integrated circuit film or forming a crystalline semiconductor film over a first substrate, as also recited in claim 15.

Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 15 and its dependent claim 16.

Claim 18 recites a method for manufacturing a semiconductor device that includes forming an element layer that includes a thin film transistor having a semiconductor layer including at least a channel forming region, a wiring connected to the thin film transistor, and an insulating film over a first substrate. The method also includes forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring; transferring the element layer from the first substrate to a second substrate so as to dispose the protruding electrode between the second substrate and the element layer; forming a thermal conductivity film on the element layer; and transferring the element layer and the thermal conductivity film from the second substrate to a sheet. The method further includes dividing the element layer into at least one integrated circuit film.

As described above with respect to claims 11 and 15, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests dividing the element layer into at

least one integrated circuit film, or transferring the element layer and the thermal conductivity film from the second substrate to a sheet, as recited in claim 18.

In addition, as described above with respect to claim 15, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring or transferring the element layer from the first substrate to a second substrate so as to dispose the protruding electrode between the second substrate and the element layer, as also recited in claim 18.

Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 18 and its dependent claim 19.

Claim 21 recites a method for manufacturing a semiconductor device that includes forming a crystalline semiconductor film over a first substrate and forming an element layer that includes an element using the crystalline semiconductor film, a wiring for transmitting an electrical signal to the element, and an insulating film. The method also includes forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring; transferring the element layer from the first substrate to a second substrate so as to dispose the protruding electrode between the second substrate and the element layer; forming a thermal conductivity film on the element layer; and transferring the element layer and the thermal conductivity film from the second substrate to a sheet. The method further includes dividing the element layer into at least one integrated circuit film. The method also includes electrically connecting the integrated circuit film to an electrode of a wiring board by the protruding electrode, and removing the sheet from the integrated circuit film.

As discussed above, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests transferring the element layer and the thermal conductivity film from the second substrate to a sheet, dividing the element layer into at least one integrated circuit film, using a crystalline semiconductor film, forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring, or transferring the element layer from the first substrate to a second substrate so as to dispose the protruding electrode between the second substrate and the element layer.

Additionally, the Examiner, as best understood, relies on Sayyah or Ding as inherently disclosing electrically connecting the integrated circuit film to an electrode of a wiring board by

the protruding electrode because the device must be mounted to be used. Even assuming that Sayyah or Ding inherently discloses a need to mount a device, neither Sayyah nor Ding describe or suggest doing so in the manner recited in claim 21 – namely, electrically connecting the integrated circuit film to an electrode of a wiring board by the protruding electrode. As noted above, neither Sayyah nor Ding describe or suggest forming a protruding electrode over the element layer for transmitting an electrical signal to the wiring, and necessarily cannot describe or suggest electrically connecting the integrated circuit film to an electrode of a wiring board **by the protruding electrode**, also as recited in claim 21 (emphasis added).

Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 21 and its dependent claims 24 and 26.

Claim 29 recites a method for manufacturing a semiconductor device that includes forming a crystalline semiconductor film over an insulating substrate and forming an element layer that includes an element using the crystalline semiconductor film, a wiring for transmitting an electrical signal to the element, and an insulating film. The method also includes transferring the element layer from the insulating substrate to a substrate, transferring the element layer to a sheet, and dividing the element layer into at least one integrated circuit film.

As described above, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests dividing the element layer into at least one integrated circuit film or a crystalline semiconductor film, as recited in claim 29.

Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 29 and its dependent claim 30.

Further, claims 12, 16 and 19 each recite that the protruding electrode is formed before transferring the element layer to the second substrate. While Ding discloses a metal protusion, Ding does not describe or suggest transferring the element layer to a second substrate, nor does the rejection contend that Ding does so. As such, neither Sayyah, Ding, nor any proper combination of the references, describes or suggests forming the protruding electrode before transferring the element layer to the second substrate.

Therefore, for this additional reason, applicant requests reconsideration and withdrawal of the rejection of claims 12, 16 and 19.

Applicant submits that all claims are in condition for allowance.

It is believed that all of the pending issues have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this reply should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this reply, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Pursuant to 37 CFR §1.136, applicant hereby petitions that the period for response to the action dated April 7, 2006, be extended for one month to and including August 7, 2006.

The fee in the amount of $120.00 in payment for the Petition for Extension of Time fee is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: August 7, 2006

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